In the Claims

Cancel claims 1-56

New Claims

Add claims 57-116 as follows:

57. A field effect transistor comprising:

a pair of source/drain regions having a channel region positioned therebetween; and

a gate positioned operatively proximate the channel region, the gate comprising semiconductive material conductively doped with at least one of a p-type or n-type conductivity enhancing impurity effective to render the semiconductive material electrically conductive, a silicide layer and a conductive diffusion barrier layer to diffusion of p-type or n-type conductivity enhancing impurity, the conductive diffusion barrier layer comprising TiW_xN_y.

58. The transistor of claim 57 wherein the conductive diffusion barrier layer comprises W_xN_y.

59. The transistor of claim 57 wherein the conductive diffusion barrier layer comprises TiO_xN_y.

60. The transistor of claim 57 wherein the conductive diffusion barrier layer is formed over the silicide layer.

61. The transistor of claim 57 wherein the silicide layer is formed over the conductive diffusion barrier layer.

62. Integrated circuitry comprising:

a field effect transistor including a gate, a gate dielectric layer, source/drain regions and a channel region; the gate comprising semiconductive material conductively doped with a conductivity enhancing impurity of a first type and a conductive diffusion barrier layer to diffusion of first or second type conductivity enhancing impurity; and

insulative material received proximate the gate, the insulative material including semiconductive material provided therein in electrical connection with the gate, the semiconductive material provided within the insulative material being conductively doped with a conductivity enhancing impurity of a second type, the conductive diffusion barrier layer of the gate being provided between the gate semiconductive material and the semiconductive material provided within the insulative material.

63. The integrated circuitry of claim 62 wherein the first type is n and the second type is p.

64. The integrated circuitry of claim 62 wherein the first type is p and the second type is n.

65. The integrated circuitry of claim 62 wherein the gate also comprises a conductive silicide.

66. The transistor of claim 65 wherein the silicide and the conductive diffusion barrier layer comprise the same metal.

67. The integrated circuitry of claim 62 wherein the semiconductive material within the insulating material contacts the conductive diffusion barrier layer of the gate.

68. The integrated circuitry of claim 62 wherein the semiconductive material within the insulating material does not contact the conductive diffusion barrier layer of the gate.

69. The integrated circuitry of claim 62 wherein the gate also comprises a conductive silicide, the semiconductive material within the insulating material contacting the silicide.

70. The integrated circuitry of claim 62 wherein the conductive diffusion barrier layer is received over the gate semiconductive material, and the semiconductive material within the insulating material is received over the gate.

71. The integrated circuitry of claim 62 wherein the insulative material comprises an opening within which the semiconductive material therein has been provided, the opening being substantially void of any conductive diffusion barrier layer material.

72. The transistor of claim 62 wherein the conductive diffusion barrier layer is selected from the group consisting of W_xN_y, TiO_xN_y, and TiW_xN_y, and mixtures thereof.

73. The transistor of claim 72 wherein the conductive diffusion barrier layer comprises W_xN_y.

74. The transistor of claim 72 wherein the conductive diffusion barrier layer comprises TiO_xN_y.

75. The transistor of claim 72 wherein the conductive diffusion barrier layer comprises TiW_xN_y.

76. The transistor of claim 62 wherein the conductive diffusion barrier layer is formed over the silicide layer.

77. The transistor of claim 62 wherein the silicide layer is formed over the conductive diffusion barrier layer.